Localized TIM Characterization Using Deconstructive Analysis

By Phillip Fosnot and Jesse Galloway
Amkor Technology, Inc.
1900 South Price Road
Chandler, AZ 85286
Phillip.Fosnot@amkor.com

Abstract

Characterizing the thermal performance of thermal interface materials (TIMs) continues to be a challenge for flip chip ball grid array (FCBGA) packages. Steady-state methods have been studied extensively but due to the difficulty in making accurate case temperature measurements have accuracy limitations. Transient measurement techniques offer an attractive alternative to steady state. However, the implementation of a property extraction analysis is more difficult to perform for thermal die with discrete heater cells as found in this study. An experimentally based deconstruction method is presented to predict the local thermal resistance of TIMs as a function time and position on the die over a short pulse ranging from 0.7ms to 100ms. The model is developed for a particular TIM but can be extended to other TIMs following the proposed calibration procedure.

Keywords

TIM, Theta JC, Transient, TTV, deconstruction

Nomenclature

A	Area (mm^2)
b	Diode calibration y-intercept (°C)
k	Thermal conductivity (W/m*K)
m	Diode calibration slope (°C/V)
P	Power (W)
R	Resistance (°C/W)
r	Radius measured from die center (mm)
t	Time (ms)
T	Temperature (°C)
V	Voltage (Volts)
Z	Impedance (°C/W)

Subscript

C	Case
J	Junction
0	Initial
th	Thermal

Greek

α	Thermal diffusivity (mm^2/s)
Δ	Change
ε	Impedance scaling based on location
τ	Time constant (seconds)
θ	Resistance (°C/W)
ζ	Impedance scaling based on time

1. Introduction

Theta JC is a thermal metric used to characterize thermal performance of high power density electronic packages ranging from automotive to high speed telecommunication applications. A quantitative expression is required to predict the temperature rise from the silicon die to the external surface of the package. Design engineers use this metric to estimate maximum power levels. Manufacturing engineers use Theta JC to track reliability of the thermal interfaces while optimizing assembly processes to track thermal performance during reliability testing. Unlike the measurement of property data, such as thermal conductivity, Theta JC is a function of the package design, manufacturing processes and the property of the thermal interface material. Therefore, when evaluating new TIMs or assembly processes, measurements should be made on actual packages to quantify the benefits compared to the existing plan of record.

A thermal performance metric requires the development of a model that characterizes the heat flow from the junction to the case. The veracity of the thermal model will determine the accuracy of the thermal measurements. Theta JC as defined in Equation (1) follows directly from the one-dimensional steady-state model. Shown in Figure 1 is a cross-section of a power amplifier assembled in a TO-220 style package. Knowing the case temperature, junction temperature, and the applied power, Equation (1) may be used to evaluate the junction-to-case thermal resistance. Thermal designers may use this equation to predict the junction temperature when operating under different power conditions and with different heat sink designs.

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad (1)$$

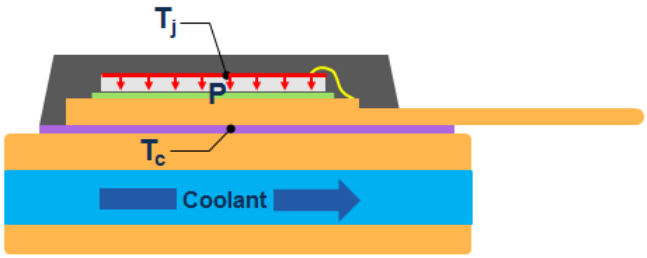


Figure 1: One-dimensional heat flow package.

Measuring the junction temperature is straightforward using a diode found on many functional die and all thermal test-die. Likewise, the power may be determined by current and voltage readings on the die. Accurate case temperature measurements are extremely challenging to make in practice.

Errors result from four sources. First, the sensor itself has inherent uncertainties. Second, the sensor may change with time as it becomes stressed after repeated testing. Third the sensor may interfere with the heat flow path at the location where the measurement is desired. Fourth and most significant is the sensor will respond to a temperature between the "true" case and the cold plate temperatures due to the large temperature gradients in TIMs. The deviation from the "true" case temperature will be a function of the sensor design and location.

To avoid many of the aforementioned concerns, several studies [1] [2] [3] have proposed transient methods to measure resistance using structured functions, which plot thermal capacitance as a function of resistance. The graph can be used to associate changes in resistance with an interface or package structure such as die, die attach, lead-frame, etc. A similar approach by Yang [4] proposes powering heaters with sinusoidal power and plotting change in phase between input power and temperature responses as a function of resistance. The central question is whether these models enable the accurate extraction of TIM resistance or Theta JC for the FCBGA packages considered in this study.

FCBGAs have a three-dimensional temperature distribution, whereas the TO-220 style package produces more of a one-dimensional temperature distribution. An experimental study [5] using a package design similar to Figure 2 is able to extract resistances using a structure function analysis; however all heaters in the die are powered simultaneously. There is uncertainty whether the structure function analysis will accurately capture the TIM resistance for the FCBGA configuration shown in Figure 2, particularly due to the discrete die heaters. An alternative method, similar to [6], is used to experimentally extract TIM resistance using a simple algebraic model that captures the temperature response as a function of power, location on the die, TIM resistance, and time.

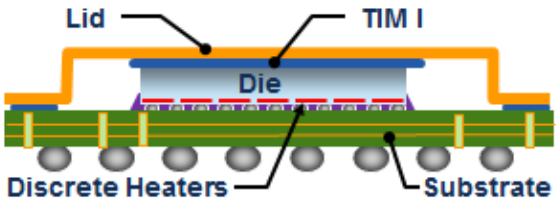


Figure 2: FCBGA Cross-section.

2. Experimental Study

The experimental test vehicle (TTV) employed in this study is a lidded FCBGA, with specs as given in Table 1. The TTV die is divided into a 7x7 array with each cell having dimensions of 2.54mm x 2.54mm. There are two heaters per cell measuring 0.9mm x 1.9mm and are symmetrically positioned about the cell's center. The temperature sensor is located in the center of each cell. The total die size is 17.8mm x 17.8mm. Figure 3 shows the test vehicle with the numbering scheme used to identify each unit cell in the array. It is convenient from a manufacturing point of view to design unit cells at a relatively small size (e.g. 2.54mm x 2.54mm). This allows larger die sizes to be fabricated by dicing the wafer in multiples of the unit cell. For example, a 5x5 array produces a die size of 12.7mm x 12.7mm and a 4x4 produces a die size of 10.2mm x 10.2mm.

Table 1: TTV Description.

Body	45mm x 45mm
Die	17.8mm x 17.8mm x 0.63mm (7x7 array heaters)
Pitch (mm)	1.0mm
Ball / Lead Count	1935
Lid	1.00mm thick nickel / copper
TIM A	K = 3.5 W/m*K (BLT ~ 40µm)
TIM B	K = 1.0 W/m*K (BLT ~ 35µm)

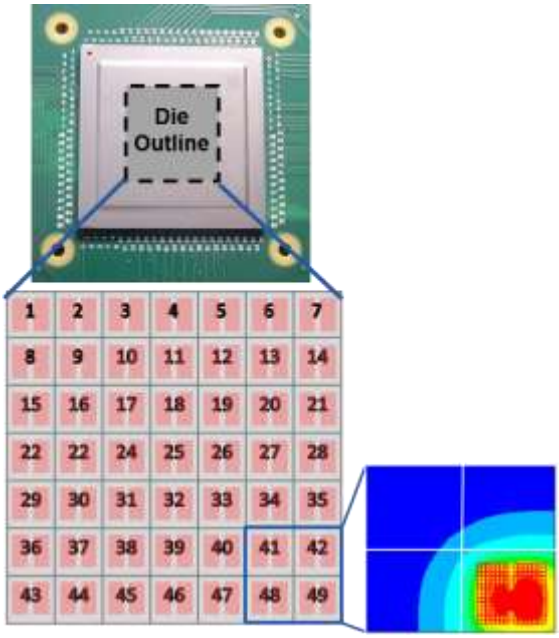


Figure 3: TTV mounted to motherboard.

What is convenient from a manufacturing point of view becomes a challenge from a thermal analysis point of view. Discrete heaters create a non-uniform temperature field as shown when one or more cells are powered. See for example in Figure 3 when corner cell #49 is powered at 4W for 100ms. A simplified thermal analysis, such as a transient one-dimensional conduction analysis, will not properly predict how the thermal resistance of the TIM layer affects the die temperature. However, one advantage for using discrete heaters instead of one large heater is that they enable an analysis to be performed on the variation of TIM resistance as a function of position on the die. By powering individual heaters one at a time, local abnormalities in the TIM may be detected more easily. For example, if manufacturing processes are not properly controlled during package assembly, the TIM may detach in the corners of large die (i.e. particularly sizes larger than 20mm x 20mm). By powering discrete cells one at a time and simultaneously measuring the temperature

response, it is possible to map out the thermal resistance in various regions of the die such as at the center #25, corner #43 or at the edge #46.

Experimental tests are run as follows. First the TTV is mounted onto the Theta JC fixture, Figure 4. Second, a pneumatic ram applies a force of 10 lbs. (44.5N) to hold the package against the cold plate. After waiting approximately 5 minutes to make certain the package is in thermal equilibrium with the cold plate, power pulses are applied to each cell one at a time while measuring the temperature rise over a 1.5 second interval, Figure 5. A time delay of approximately 5 seconds is imposed between cell tests to allow the die to return to the original cold plate temperature. In order to accurately capture the transient response, data are collected at 10,000 Hz, yielding data every 0.1 millisecond during the heating process. Figure 5 presents sample data collected from one cell during a test. The temperature versus time curve shows heating during the application of a 1.0 second power pulse and cooling thereafter. A complete package test consists of powering cell #1-49 successively. Three types of raw data are gathered during the tests; diode voltage, shunt resistor voltage, and heater voltage drop using four-point leads. Direct current power dissipated to each individual heater is calculated with the current and heater voltage drop. Temperature of the cell is calculated by applying a linear equation to the diode voltage data, according to Equation (2). Coefficients m and b are the temperature-sensitive parameters of the diode determined beforehand during a calibration process. Only the slope m is necessary in this study since only the temperature difference from the initial preheated state is required, Equation (3).

$$T_{heater} = m * \Delta V_{diode} + b \quad (2)$$

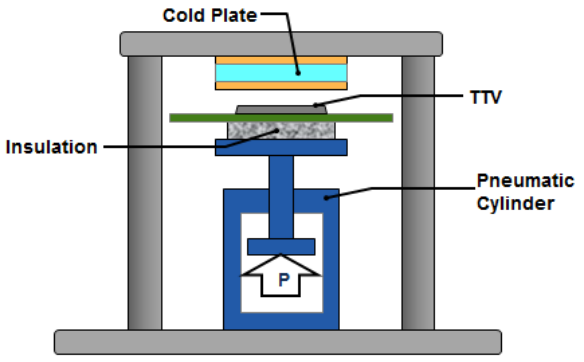


Figure 4: Theta JC test fixture.

By dividing the change in temperature by applied power, a thermal impedance curve is calculated, allowing a meaningful comparison of multiple heating curves regardless of their dissipated power levels. Transient test data are generated by recording the temperature response of the TTV to a power step function. Thermal impedance, Z_{th}, versus time data are collected to generate a heating curve for later analysis. These data are recorded in the form of Z_{th} versus time according to Equation (3).

$$Z_{th}(t) = \frac{T(t)-T_0}{P} = \frac{m\Delta V_{diode}}{P} \quad (3)$$

A deconstruction experiment is conducted by making thermal measurements with and without the lid to understand the transient contributions of the die compared to the full package.

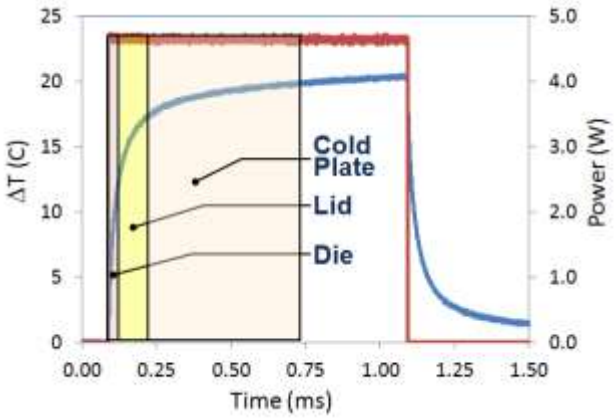


Figure 5: Transient temperature response to a power input square wave.

Packages are solder mounted to the motherboard. Thereafter, the lids are removed by cutting the lid seal epoxy between the lid and substrate. The original TIM I is cleaned from the die and lid surface. The lid is reused by manually applying the desired TIM I material and pressing the lid down in position. The lid is held in place using the force of the Theta JC fixture. Two grease style TIMs are used for this study; TIM A (k = 3.5 W/m*K, BLT ~ 40µm), TIM B (k = 1.0 W/m*K, BLT ~ 35µm). An extremely high resistance TIM II (paper sheet, R > 1000C/W*mm^2) is used as a reference condition to detect when the heat wave passes through the die (without lid test) or through the lid (with lid test) and into the cold plate. The experimental conditions selected for this study are reported in Table 2. Measurements are made at all cell locations, cells 1-49.

Table 2. Test Conditions.

Test	Package	TIM I	TIM II
1	Without Lid	N/A	TIM A
2	Without Lid	N/A	Paper
3	With Lid	TIM A	TIM A
4	With Lid	TIM A	Paper
5	With Lid	TIM B	TIM A
6	With Lid	TIM B	Paper

Figure 6 presents data for tests 1–4. Upon initial inspection, each curve looks identical until approximately 0.7 ms. At this point, the bare die / paper TIM II, test 2, separates from the bare die / TIM A, test 1. Since the configurations are identical except for the TIM II material, the separation point of the Z_{th} curves at ~1.3 C/W infers the resistance associated with the bare die case. By adding another two data sets to the

plot, tests 3 and 4, the same method is applied to find the thermal resistance of the die, TIM I and the lid. By visual approximation, the curves diverge at about 100 ms, with a Z_{th} ~2 C/W.

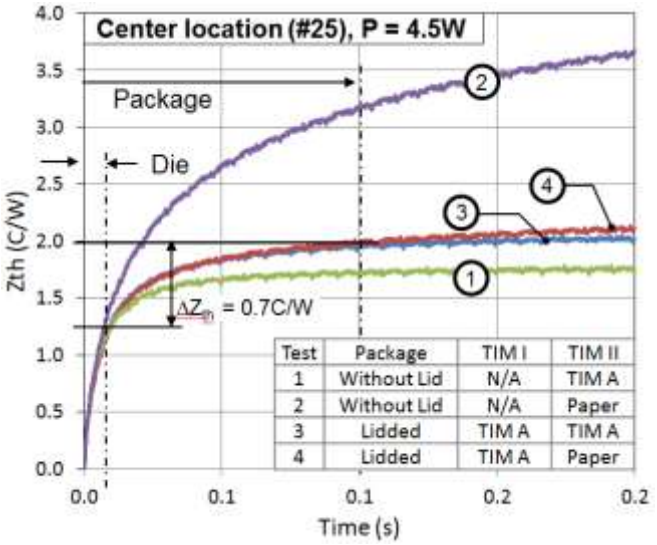


Figure 6: Sample deconstruction plot, center cell. Four package configurations generate 4 unique temperature traces.

A simplistic model is considered first by taking the difference between the Z_{th} curve for the without lid test from the Z_{th} curve with lid test. Doing so yields a ΔZ_{th}~0.7C/W based on the measurements reported in Figure 6. As a reality check, ΔZ_{th} is then compared to the resistance of TIM A. If one approximates the heat transfer area equal to an individual cell 6.45mm^2, then the resistance times cell area is approximately 4.5C/W*mm^2. This is approximately 2 to 3 times lower than the manufacture rated value for the TIM resistance. Hence a simple deconstruction analysis, based on the resistance equal to ΔZ_{th}*effective heat transfer area of the heated cell, does not produce a meaningful TIM I resistance.

Since the deconstruction analysis for the TTV does not produce correct absolute TIM I resistance, a relative comparison is then made between the two TIM I materials to determine if the correct trends are produced, Figure 7.

Based on a one-dimensional model, (i.e. R*A = BLT/K), TIM B should have approximately 3X higher resistance then TIM A. In a qualitative sense, TIM B has a higher Z_{th} compared to TIM A but in an absolute sense the difference is smaller than what is expected considering TIM B has more than three times higher thermal resistance compared to TIM A.

Experimental data are also collected comparing the Z_{th} curves at the corner (#43), center (#25), edge (#46) and at the mid-point (#37) for test condition 3 (i.e. lidded package with TIM A both at TIM I and TIM II interfaces). As shown in Figure 8, the center and mid-point locations have similar impedance curves, the edge location having the next higher and the corner having the highest impedance. The corner has higher die spreading resistance since the heat can only spread in two directions.

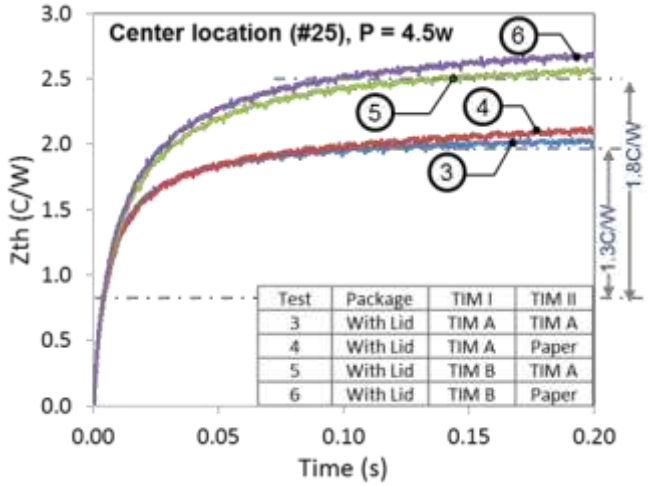


Figure 7: Effect of TIM material.

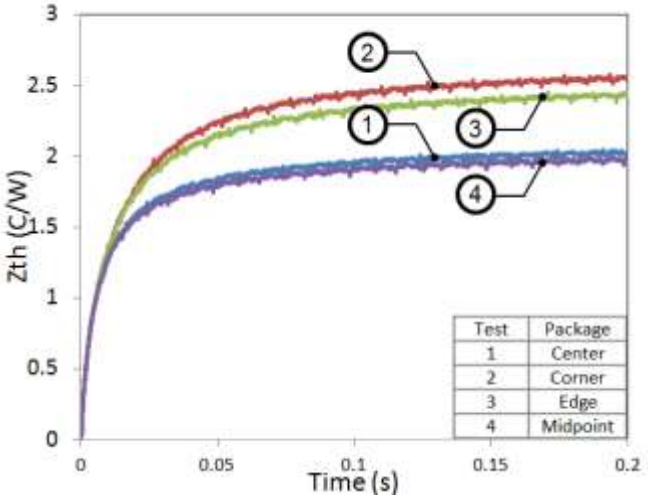


Figure 8: Difference in Zth as a function of location.

Zth curves compared to a reference material show a consistent shape. The reference curve can be used as an indicator for a shift in thermal performance from accepted manufacturing limits.

For example, the lid is purposely assembled in a tilted configuration, Figure 9, by placing a 75µm shim underneath one side of the foot. As expected, the Z_{th} curves increased on the edge with the largest BLT, cell #28, and the lowest curve was observed at cell # 23, Figure 9. Cell #22 had the second highest Z_{th} curve since it was on the opposite edge.

3. Modeling

Experimental modeling observations are used to develop a transient model as a function of cell position, time and local resistance in the form of Equation (4).

$$Z|_{th} = f(time, location, R_{TIM}) \qquad (4)$$

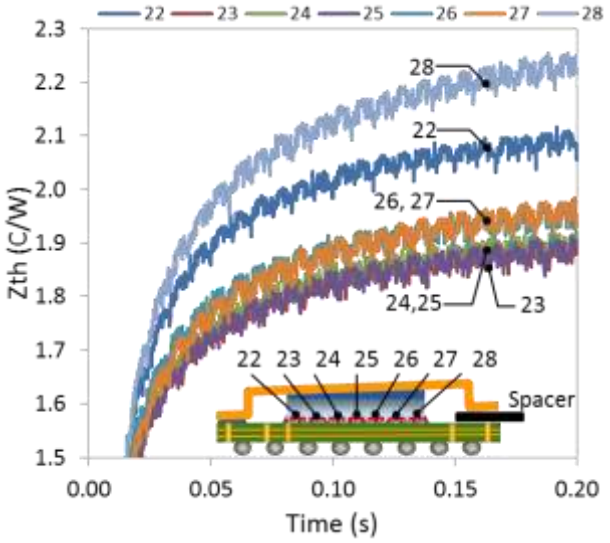


Figure 9: Effect of lid tilt.

Essentially, the conduction analysis may be treated as an inverse problem with the goal of extracting material properties along the heat flow path, knowing the die temperature and applied heat. This type of analysis is similar in many respects to seismic imaging technology used to locate oil or natural gas during geological surveys [7]. By adjusting the material properties in the model such that the transient predictions match the experimental data, one may estimate interfacial resistances such as TIM I and TIM II.

Unlike the steady-state measurement method represented in Equation (1), a model of the transient heat flow must be applied and the materials extracted indirectly. One of the more popular techniques used to model the transient thermal response makes use of an electrical analogy, a resistor and capacitor network. Here the steady state components are modeled as resistors, R_i, and the transient components are modeled as capacitors, C_i. The electrical network shown in Figure 10 is a Cauer network. It has been studied extensively in applications for thermal networks [8].

Numerical values for the resistances and capacitors may be determined by fitting the solution of the circuit with values that best represent the experimental transient data. For the case of one element, the junction temperature may be predicted following the lumped thermal mass solution for a constant heat flux with convection.

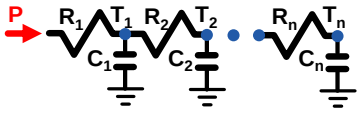


Figure 10: Thermal resistor network.

$$Z_{th} = \frac{T_J - T_C}{P} = R\left(1 - e^{-t/\tau}\right) \quad (5)$$

For large times, Equation (5), Z_{th} has the same form as Theta JC. More terms may be added to Equation (5) to account for additional components or interfaces in the heat flow path operating on different time scales [9]. For the configuration shown in Figure 10, three terms are sufficient to fit the experimental data. In theory, the first term represents the die with a short time constant τ_1. The second term represents the die attach material between the die and lead frame. The last term represents the lead frame, which has a much longer time constant, τ_3.

$$Z_{th} = \zeta(t) = R_1\left(1 - e^{-\frac{t}{\tau_1}}\right) + R_2\left(1 - e^{-\frac{t}{\tau_2}}\right) + R_3\left(1 - e^{-\frac{t}{\tau_3}}\right) \quad (6)$$

Another model for Z_{th}, Equation (7), can be made by approximating the heat flow as one-dimensional conduction into a semi-infinite solid with a constant wall heat flux boundary condition [10, 11].

$$\frac{T_J - T_C}{P} = \frac{1}{A\,k}\left[\sqrt{\frac{4\alpha t}{\pi}}\right] \quad (7)$$

There are more complex analytical formulations that consider the effect of heated area and multi-layer media [12]. Yet it is unlikely that these more advanced analytical conduction analyses will yield explicit relations to enable the extraction of material properties.

Experimental data are compared to three different fits represented by Equations (5), (6) and (7), Figure 11. A simple one rung Cauer network, Equation (5), will not fit the experimental data well at all. Adding two additional rungs as represented by $\zeta(t)$ in Equation (6) provides a close fit. $\zeta(\tau)$ is used in section 3 as a general fit for the time dependency of Z_{th}. The optimized constants given in Table 3 do not represent material properties. The one-dimensional semi-infinite solid solution, Equation (7), does not fit the data either even at small times due to the three-dimensional conduction nature of this problem.

Table 3: Z_{th} curve fit constants.

Equation (5)	Equation (6)	Equation (7)
R = 1.97	R_1 = 0.583	1/(A*k) = 0.33
τ = 0.012	τ_1 = 0.0021	(4α/π) = 1533
	R_2 = 0.996	
	t_2 = 0.00996	
	R_3 = 0.457	
	τ_3 =0.0586	

Because of the complex boundary conditions and the multilayer construction of the FCBGA package, closed form solutions are not very accessible. Finite element analysis (FEA) will yield transient solutions for complex domains with limited restrictions but requires simulations for each case of interest [6].

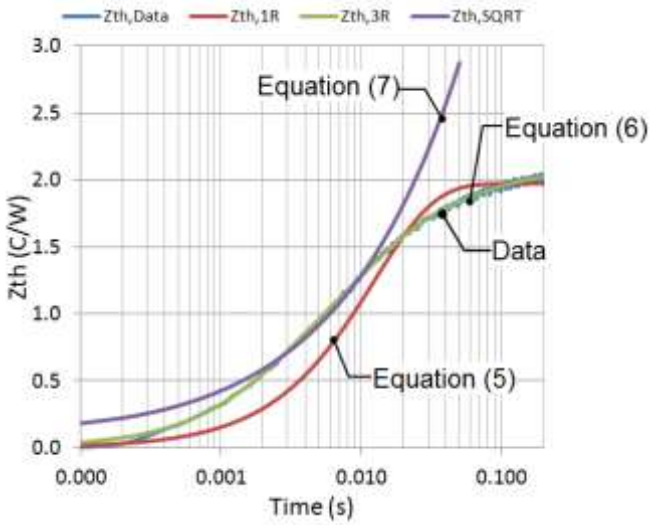
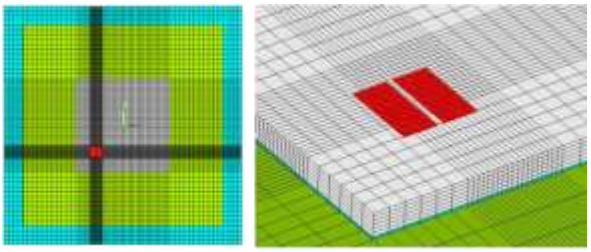
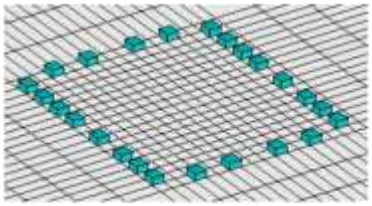


Figure 11: Z_{th} models compared to data.

A FEA model is developed for a FCBGA package shown in Figure 12(a) with the lid hidden from view to make the die visible. The model is able to study in detail the thermal transient with fine mesh at the location where the heat is applied, Figure 12(b). The model also includes the bump features in detail to more accurately capture heat flowing to the substrate, Figure 12(c). Fortunately for this study, the bump density is very small, approximately 90% less, in comparison to functional packages. Therefore, the heat flow to substrate is less than 5% of the heat flowing into the die.



12 (a) 12 (b)



12 (c)

Figure 12: FEA model details. 12(a): Top view of the package with lid hidden. 12(b): Close up view of die with applied heat load. 12(c): Bump geometry on the active side of die.

Shown in Figure 13 is the temperature versus time plot for the lidded package with TIM A for the heat spot at the corner location #43 and center location #25 after 50ms with an applied power of 4.0W. A steeper temperature response is seen for the corner compared to the center which is similar to experimental data shown in Figure 8.

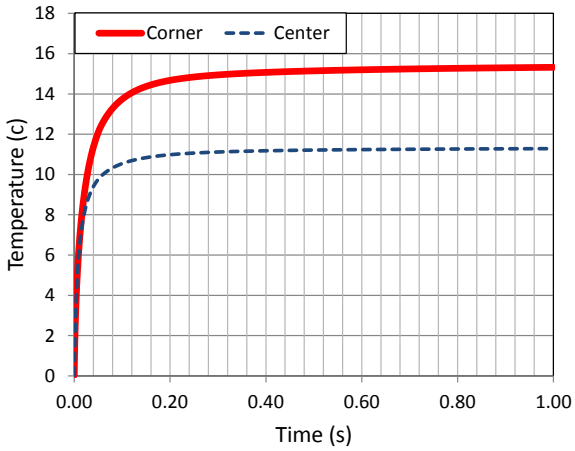
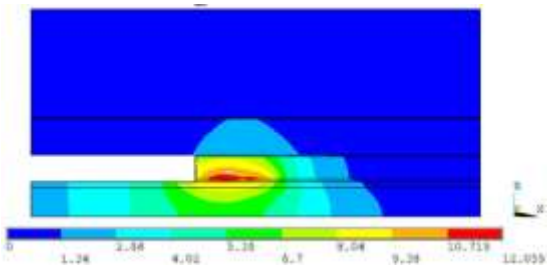
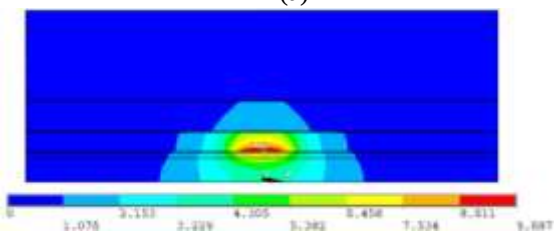


Figure 13: Lidded package transient response as a function of cell location. Corner is located at #43 and center at #25.

The impact of heat constriction in the corner cell is clearly shown in Figure 14. Heat applied to the center region can spread laterally in four directions whereas heat applied to the corner can spread laterally in only two directions and is essentially insulated on the edges of the die.



14 (a)



14 (b)

Figure 14: Model isotherms through (a) corner cell and (b) center cell.

Simulations are run for the center cell with an applied power of 4.0W using TIM A over a range of resistances. When the TIM resistance is increased from a reference value of 10C/W*mm^2 to 50C/W*mm^2, the Z_{th} curve shifts upward a proportional amount. The predicted curves in Figure 15 are similar and may be scaled to provide a linear offset based on the local resistance. To scale the effect of Z_{th} with respect to radius from die center, r, a model is fit to experimental data to

account for higher resistances in the corner and along edges of the die, Equation (8).

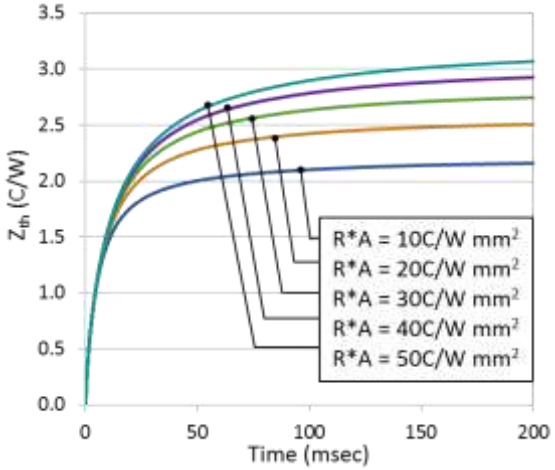


Figure 15: Effect of resistance of TIM on transient response.

$$\varepsilon(r) = [1 + 0.018 * r^{1.1}] \quad (8)$$

A combined Z_{th} model is presented in Equation (9) including time scaling, Equation (6), and location scaling, Equation (8) where R_{ref} is a known resistance calculated from a reference TIM material.

$$Z_{th,model}(t,r) = \varepsilon(r) * \zeta(t) * R_{ref}; \quad 0.7msec < t < 200msec \quad (9)$$

The resistance for an unknown TIM at a particular location may be calculated from Equation (9) using the experimental Z_{th} curve as follows in Equation (10).

$$R_{TIM}(r) = \frac{R_{ref}}{\varepsilon(r) * (200 - 0.7)} \int_{0.7}^{200} \frac{Z_{th}}{\zeta(t)} dt; \quad 0.7msec < t < 200msec \quad (10)$$

The TIM resistance for a particular location r is determined by averaging the ratio of Z_{th} to the scaled time function $\zeta(t)$ over the time range from 0.7 to 200ms and scaled by the location function $\varepsilon(r)$. The TIM resistance extraction procedure is listed below.

1) Choose a reference material, such as thermal grease, with a low enough viscosity that will spread evenly while still holding its shape. A liquid TIM material would not be a suitable candidate due to its low viscosity. Nor would a phase change material, since its high viscosity would not allow adequate flow.
2) Load the TTV with lid on the Theta JC fixture and measure the Z_{th} curve.
3) Fit the experimental constants to Equation (6) for several different cells near the die center.
4) Determine the position scaling constants in Equation (8) using Z_{th} curves at different locations.
5) Combine time and location scaling into Equation (9). Local resistance may be determined using Equation (10) for a new material.

To test how Equation (10) correlates with changes in resistance, simulation data presented in Figure 15 are evaluated for several different TIM resistance values. The correlation between the average change in Z_{th} versus TIM resistance is quite good as shown in Figure 16. Zth curves can be scaled with a reference condition to estimate resistances for an unknown TIM or predict how TIMs degrade during reliability tests.

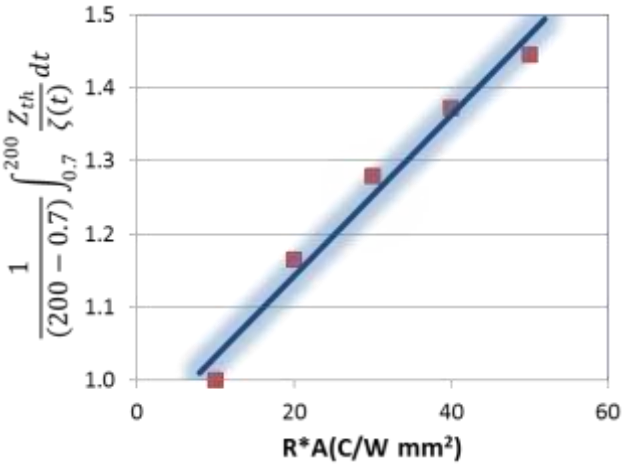


Figure 16: Experimental data compared to model.

4. Conclusions

Due to the highly three-dimensional temperature profile present in a test chip powered by individual heaters, an analytical solution is not found to adequately characterize TIM resistances. Modeling trends observed from FEA transient temperature curves give insight into modeling TIM resistance using an algebraic equation including transient scaling and location scaling. The model is calibrating with a known reference condition that could then be used to analyze the performance of new TIMs or be used to detect manufacturing abnormalities.

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